

out the present disclosure. As will be realized, the present disclosure is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, all without departing from the present disclosure. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawing and in which like reference numerals refer to similar elements and in which:

FIGS. 1 through 8 illustrate, in cross sectional view, a process flow to produce a finFET RMG structure, in accordance with an exemplary embodiment.

DETAILED DESCRIPTION

In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of exemplary embodiments. It should be apparent, however, that exemplary embodiments may be practiced without these specific details or with an equivalent arrangement. In other instances, well-known structures and devices are shown in block diagram form in order to avoid unnecessarily obscuring exemplary embodiments. In addition, unless otherwise indicated, all numbers expressing quantities, ratios, and numerical properties of ingredients, reaction conditions, and so forth used in the specification and claims are to be understood as being modified in all instances by the term "about".

Still other aspects, features, and technical effects will be readily apparent to those skilled in this art from the following detailed description, wherein preferred embodiments are shown and described, simply by way of illustration of the best mode contemplated. The disclosure is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

Adverting to FIG. 1, fins **101** are formed over substrate **103**. Substrate **103** includes a Si substrate. Other examples of materials that may be suitable for use in the substrate **103** include silicon-on-insulator (SOI), silicon germanium (SiGe), germanium (Ge), and/or compound semiconductor materials. Processes, such as photolithography and etch processes, can be used to create the fins **101**. The fins **101** may include silicon. Fins **101** include a dielectric layer **105** deposited over the surface of the fins **101** and substrate **103**. The dielectric layer **105** is a high-k dielectric material. In FIG. 1 shallow trench isolation (STI) regions **107** are formed in the substrate **103** between the fins **101**. The STI is formed by etching a pattern of trenches in the substrate **103**, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches, and removing the excess dielectric.

Prior to the deposition of the dielectric layer **105**, the substrate undergoes a conventional processing for a bulk finFET. For example, shallow trench isolation (STI) regions and fins are formed by multi-layer hard mask deposition, STI/fin hard mask patterning, etching, photoresist stripping, Si-etching, oxide gap-fill, CMP, annealing, and hard mask removal. A thin oxide is grown to 1 nm over the fins **101**. Next, n⁺/p⁺ well patterning; n⁺/p⁺ implanting; and annealing are performed. The gate stack is then formed by polysilicon deposition and patterning; spacer formation; and halo

implants (selective for n⁺/p⁺ core, static random-access memory (SRAM), and input/output (I/O) areas). Epitaxially grown SiGe (for p-type source/drain) with in-situ or p⁺ implant doping, and Si-epitaxy (for n-type raised source/drain) with in-situ n⁺ implant doping are performed. Next, replacement metal gate (RMG) formation is performed. An interlayer dielectric (ILD) is deposited followed by polysilicon open CMP; and polysilicon removal. The dielectric layer **105** is then deposited over the fins **101**.

In the example of FIG. 2, the fins **101** have a first metal **201** deposited thereon. The first metal **201** can include metal compounds such as Mo, Cu, W, Ti, Ta, TiN, TaN, NiSi, CoSi, and/or other suitable conductive materials. The first metal **201** is deposited to a thickness of 0.1 to 10 nm.

Adverting to FIG. 3, an isolation material **301** is deposited over and between the fins and subjected to CMP to planarize the upper surface of the isolation material **301** down to an upper surface of the first metal **201**. The isolation material **301** can include an OPL. The isolation material **301** can be spin coated over the first metal **201**.

Adverting to FIG. 4, the isolation material **301** is recessed to expose an upper region of the first metal **201** and fins **101**. Upper regions of each the first metal **201**, fins **101** and the dielectric layer **105** are exposed following the recessing of isolation material **301**.

Turning to FIG. 5, the first metal **201** is etched down to the isolation material **301**. Following the etching of the first metal **201**, the upper portion of each of the fins **101** and dielectric layer **105** are exposed. Adverting to FIG. 6, the remaining portion of the isolation material **301** is removed to expose a lower portion of the first metal **201**. The isolation material **301** can be removed by wet etching.

In the example of FIG. 7, a second metal **701** is deposited. In particular, the second metal **701** is formed over the first metal **201** and over the dielectric layer **105** adjacent to an upper portion of each of the fins **101**. The second metal **701** can include metal compounds such as Mo, Cu, W, Ti, Ta, TiN, TaN, NiSi, CoSi, and/or other suitable conductive materials. The first metal **201** is deposited to a thickness of 0.1 to 10 nm. The second metal **701** is different than the first metal **201** and the WF of the first and second metals is different. The first metal **201** has a lower work function than the second metal **701**.

FIG. 8 illustrates an alternative process flow in which a metal cap layer **801** is formed. The metal cap layer is formed between the first metal layer **201** and second metal layer **701**, adjacent to a lower portion of each of the fins **101**. The metal cap layer **801** is deposited over the first metal layer **201** prior to the deposition of the isolation material **301**. An upper portion of the metal cap layer **801** is removed at the same time the upper portion of the first metal layer **201** is removed to expose the upper portion of the fins **101**. The portion of the metal cap layer **801** that remains is illustrated in FIG. 8. The metal cap layer **801** is deposited to a thickness of 0.1 to 5 nm and can include metal compounds such as Al, Mo, Cu, W, Ti, Ta, TiN, TaN, NiSi, CoSi, and/or other suitable conductive materials.

Additional processing may continue for the fabrication of one or more metal gates on the substrate **103**. A metal gate **803** can be formed on and over the fins **101**, as illustrated in FIG. 8. Following the deposition of the first metal layer **201** and second metal layer **701**, a gate metal filling step is performed followed by silicide and contact formation. Silicide trench patterning and etching are performed followed by a metal deposition (e.g., nickel, tungsten) and silicide formation. Contact patterning can be performed by a double patterning process and the contact can be filled with a metal